REMARKS

Claims 1, 2, and 4-5 are pending in this application, with claims 1 and 2 amended and claims 3 cancelled herein. No new matter been added.

In the office action claims 1-5 are rejected under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter. Claim 1 is amended herein to recite physical features making it therefore concrete. Currently the claim recites one or more processors, an input data memory, an output data memory and a switching controller. Withdrawal of the rejection is requested.

On the merits, the office action rejects claims 1-5 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,805,129 to David.

As has been previously explained to the Examiner, David describes a two-dimensional space filter of m×m positioned in a compression circuit for reducing aliasing due to image compression.

However, David merely teaches an FIR filter itself having a plurality of input terminals but fails to teach or suggest any peripheral structure of the FIR filter such as processors, an input data memory, a switch table, and a switching controller as recited in claim 1, as amended. Accordingly, it is David does not teach a single digital filter (having a single input terminal) that reads the input data strings from an input data memory to be filtered and generates output data strings; an output data memory stores the output data strings generated by the digital filter; a switch table associates an address of the input data memory in which the input data strings are stored with an address of the output data memory in which the output data strings are stored; and a switching controller provides variable timings of reading the input data strings out of the input data memory based on the switch table and of writing the input data strings as the output data strings in the output data memory through the digital filter.

As described in [0038] of the specification of this patent application, the switching controller performs a switching (timing) control of reading the input data strings out of the input data memory based on the switch table and of providing the input data strings as the output data strings to the output data memory through the digital filter.

Consequently, with variable timing, by the switching controller, as claimed in claim 1, the present invention makes it possible to designate or change the sequence of filtering the input data strings based on the switch table (see [0039] of same). Such a feature is not taught by the relied upon portions of David.

Accordingly, claim 1 is believed to be patentable over David under 35 U.S.C. 102(b).

In Conclusion

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

/Nathan Weber/
Nathan Weber
Reg. No. 50,958

CUSTOMER NUMBER 026304
Telephone: (212) 940-8564
Fax: (212) 940-8986 or 8987
Docket No.: 100794-00475 (FUJZ 20.589)
NDW:cc